

**38705** Digital Trainer has been designed specifically for the study of Digital IC Circuits. Digital Trainer is a completely self contained, most versatile, sophisticated and economical. The board is absolutely self contained and requires no other apparatus.

Practical experience on this board carries great educative value for Science and Engineering Students.

**SPECIFICATIONS**

- 01 + 5V & 12V DC at 0.5Amp, IC Regulated Power Supply.
- 02 Twelve , two position toggle switches prewired to give binary logic input states.
- 03 Twelve LED logic indicators with transistor drivers.
- 04 Two digit Seven Segment Displays with decoder driver and provision to take-out output for monitoring.
- 05 Clock Generators Adjustable : (1) 0.1-10Hz ( 2) 10Hz-1KHz (3) 1KHz-100KHz with Coarse and Fine Adjustable.
- 06 Two Single pulse mono pulser.
- 07 IC BASE 8, 14, 16 Pin 2No. IC BASE 24, 28 Pin 1No. IC BASE 24, 28, 40 Pin 1No. gold/silver plated Zero. Insertion Force (ZIF) dual in line Package (DIP) on Front Panel.
- 08 Two adaptators (BNC/2) mm sockets for connection with measure instruments.
- 09 Components Provided :  
ICs-555/1, 4001/1,4008/1, 4011/1, 4013/1, 4018/1, 4027/1, 4045/1, 4098/1, 7400/1, 7402/1, 7404/1, 7407/1, 7408/1,7411/1, 7432/1, 7472/1, 7473/2, 7480/1, 7486/1, 7489/1, 7490/3, 7493/1, 7496/1, 74121/1 74181/1, 74194/1 total = 30
- 09 Accessories : Mains cord, Operating and Experimental manual, Red & Black patch cords 18 each
- 10 Instruction manual : Strongly supported by detailed operating instructions.
- 11 Wiring of all types of experiments become simple and less time consuming.
- 12 Adequate no. of other Electronic Components.
- 13 The unit is operative on 230V ±10% at 50Hz A.C. Mains.
- 14 Weight : 4.700 Kg. (Approx.)
- 15 Dimension : W415 x H165 x D 315.

**THE TRAINER COVER THE FOLLOWING EXPERIMENT LOGIC GATES**

- 01 AND GATE (DIODE & TTLLOGIC)
- 02 OR GATE (DIODE LOGIC)
- 03 NAND GATE (TTL)
- 04 NOR GATE (TTL)
- 05 NOTGATE (TTL)
- 06 EXCLUSIVE - OR GATE (TTL)

**BOOLEAN ALGEBRA**

- 07 TO PROVE BOOLEAN THEOREMS  $A + 1 = 1$
- 08 TO PROVE BOOLEAN THEOREM  $A + A \cdot B = A$
- TO PROVE DEMORGAN'S THEOREMS**
- 09  $\overline{A + B} = \overline{A} \cdot \overline{B}$
- 10  $\overline{A \cdot B} = \overline{A} + \overline{B}$



**MONOSTABLE (TTL)**

- 11 NEGATIVE EDGE TRIGGERED MONOSTABLE
- 12 SCHMITTTRIGGER

**FLIPFLOP(TTL)**

- 13 RS FLIPFLOP
- 14 CLOCKED RS FLIPFLOP
- 15 J. K. FLIP-FLOP

**BINARY COUNTERS (TTL)**

- 16 BINARY RIPPLE COUNTER
- 17 SYNCHRONOUS COUNTER

**DIVIDE BY N COUNTER**

- 18 DIVIDE BY6 COUNTER USING 7493 IC
- 19 DIVIDE BY60 COUNTER USING 7493 AND 7490 IC'S
- 20 RING COUNTER

**FULL & HALF ADDERS (TTL)**

- 21 HALF ADDER
- 22 FULLADDER

**SUBTRACTORS & ARITHMETIC LOGIC UNIT (TTL)**

- 23 HALF & FULLSUBTRACTOR
- 24 ARITHMATIC LOGIC UNIT

**REGISTERS (TTL)**

- 25 SHIFT REGISTER CONSTRUCTED FROM MASTER SLAVE JK FF
- 26 5 BIT REGISTER (USING 7496)
- 27 UNIVERSALSHIFT REGISTER

**MEMORIES (TTL)**

- 28 ORGANISATION OF RAM / IC 7489 - RAM
- 29 ROM (READ ONLY MEMORY)

**EXPERIMENT OF CMOS DEVICES**

- 30 NAND CMOS
- 31 NOR CMOS
- 32 BOOLEAN ALGEBRA(CMOS)
- 33 ASTABLE MULTIVIBRATOR & SCHMITT TRIGGER WITH ADJUSTABLE TRIGGERING (CMOS)
- 34 MONOSTABLE MULTIVIBRATOR (CMOS)
- 35 FLIPFLOPS (CMOS)
- 36 HALF & FULLADDER (CMOS)
- 37 PRESETTABLE DEVIDE-BY-N COUNTER (CMOS)
- 38 BINARYTO DECIMALCONVERSION
- 39 3 DIGITSTROKE COUNTER USING IC 7490
- 40 ACCURATE TIMER USING BELCD 4045 & CD 4013
- 41 MONOSTABLE OPERATION USING IC 555 TIMER
- 42 ASTABLE OPERATION USING IC 555 TIMER
- 43 FREQUENCY MODULATION USING IC 555 TIMER
- 44 SQUARE WAVE GENERATOR USING IC 555 TIMER

Note: Specifications are subject to change.